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Docket No.
BUR990217US1

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

Brian L. allen

For: **INTERLEAVED FINITE IMPULSE RESPONSE FILTER**

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Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EL046032163US**
- ☒ **2** sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☒ Signed. ☐ Unsigned.
- ☒ Power of Attorney
- ☒ Information Disclosure Statement
- ☐ Preliminary Amendment
- ☒ Other: **Recordation, Assignment, Acknowledgement Postcards**

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	20	- 20 =	0	x	$22.00	$0.00
Indep. Claims	3	- 3 =	0	x	$82.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
					TOTAL FILING FEE	$690.00

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  - ☒ Charge the amount of **$690.00** as filing fee.
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Dated: 1-31-00

Signature

Richard A. Henkler, Reg. No. 39,220
IBMCorporation - MailStop: 972E
1000 River Street
Essex Junction, VT 05452

Tel. No.: (802) 769-8585

cc:

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APPLICATION

FOR

UNITED STATES LETTERS PATENT

APPLICANT NAMES: Brian L. Allen

TITLE: INTERLEAVED FINITE IMPULSE RESPONSE FILTER

DOCKET NO.: BUR990217US1

INTERNATIONAL BUSINESS MACHINES CORPORATION

INTERLEAVED FINITE IMPULSE RESPONSE FILTER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to digital filters and more particularly to an improved interleaved digital filter that eliminates the need for pipeline stages and, in turn, decreases in the number of latches required in the filter, which decreases the power and space required by the filter

Description of the Related Art

Finite impulse response digital filters are commonly used to perform arithmetic operations on digital signals (samples) of data. The speed of digital filters is limited by the internal components of the filters. Generally, with full rate design conventional digital filters, one sample can be filtered per cycle. In order to process multiple samples per cycle, an interleaved (half rate) digital filter is utilized.

Interleaved digital filters receive multiple samples (odd and even samples) per cycle and process the odd and even samples in parallel. Therefore, an

interleaved digital filter can operate at twice the speed of a full rate design digital filter because the interleaved digital filter processes twice the number of samples per cycle.

However, the disadvantage of interleaved filters is that they include twice the number of multipliers, adders and storage elements when compared to full rate design digital filters. Therefore, the interleaved digital filter are twice as expensive to manufacture and twice as large as a full rate digital filters. However, the interleaved digital filters consume only about the same amount of power as the full rate digital filters because, while the interleaved design requires twice as many elements, the elements operate at half the frequency, which results in an approximately equal power consumption.

Figure 1 is a schematic diagram of a conventional direct Form 1 interleaved architecture filter. Such a filter is described in greater detail in U.S. patent No. 3,665,171, which is incorporated fully herein by reference. More specifically, Figure 1 illustrate the inputs 10, 11 for the even and odd samples. The samples are multiplied by multipliers h0-h9 after being delayed by the delay elements D. The multiplied samples are then processed through pipelines stages 12 before being added by adders 13. The pipeline stages 12 are necessary to avoid having more than two inputs is supplied to any of the adders 13 during any cycle. The pipeline stages are necessary because there is not enough time to multiply all of the samples and sum them in one cycle. A pipeline stage is used to allow the

multiplication to take one cycle and the summation of all the multiplier outputs to take one cycle. Final summation units 14 produce the odd and even filter outputs.

Since all of the multiplier h0-h9 outputs need to be summed at once, pipeline stages 12 are used. The pipeline stages 12 consists of storage elements that hold the outputs of the multipliers for one clock cycle. However, the pipeline stages 12 add an extra cycle of latency and increase the total number of storage elements. Therefore, there is a need to eliminate the pipeline stages 12 from digital filters so that the size of the filter, its associated manufacturing costs, and its power consumption can be reduced.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a structure and method of a non-recursive filter for receiving samples and generating a filtered signal. The filter includes at least one input for receiving the samples, a plurality of summation units, and a plurality of delay elements positioned between the summation units. Each of the summation units includes at least one multiplier directly connected to the input (the multiplier multiplies the samples and providing multiplied samples) and at least one adder connected to the multiplier (the adder adds the multiplied samples and provides added samples). The delay elements receive the added samples and provide a delayed output of the added

samples to a successive summation unit. Each of the delay elements is connected to an adder of the successive partial summation unit.

The non-recursive filter further comprises an initial delay element connected to an initial multiplier. The initial delay unit supplies an initial delayed sample to an adder of an initial summation unit. The multiplier receives the samples in an undelayed state. Each of the summation units may include two of the multipliers supplying the multiplied sample to a single adder.

In another embodiment, the non-recursive filter comprises a plurality of successive partial summation units, each partial summation unit having a multiplier for multiplying an undelayed state of each of the samples, an adder for adding multiplied samples, and a plurality of delay elements each coupled to the adder for receiving added samples and for providing a delayed output of the added samples to a successive partial summation unit.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a schematic diagram of a conventional interleaved digital filter;

Figure 2 is a schematic diagram of an interleaved digital filter according to

a preferred embodiment of the invention; and

Figure 3 is a schematic diagram of an interleaved digital filter according to another embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

A first embodiment of the invention is illustrated in Figure 2. As discussed with respect to Figure 1 above, the inventive structure also includes odd and even sample inputs 10, 11, multipliers h0-h9, delay elements D, adders 13, and odd and even filter outputs 14. As would be known by one ordinarily skilled in the art given this disclosure, the multipliers h0-h9 can be constructed in various ways (e.g., table lookup, sign magnitude, two's complement, etc.) without affecting the spirit of the invention. Similarly, the adders can be constructed in various ways (ripple carry, carry save, carry lookahead, etc.) and still not affect the spirit of the design. The delay blocks D include a number of storage elements where data is clocked in each clock cycle. Once again, as would be known, the delay elements D can be constructed in various ways (D flip flops, latches, etc.) and still not affect the invention. For a given sample input, x0, x1, x2, x3, x4, x5...., the even sample input 10 is commonly referred to as x0, x2, x4... and the odd sample input 11 is referred to as x1, x3, x5...

However, while the invention includes many of the same basic elements shown in Figure 1, the invention is fundamentally different than conventional structures because the invention eliminates the pipeline stages 12. More specifically, since all the multiplier outputs are summed between delay elements, together at once, a pipeline stage 12 is not needed. This allows the latency of the inventive architecture to be one less than the structure shown in Figure 1 and requires less storage elements than Figure 1. Therefore, the invention is smaller, less expensive to produce, and consumes less power than conventional filters, such as the one shown in Figure 1.

As shown in Figure 2, the invention relocates the delay units D such that the delay units D are positioned between the adders 13. Further, the multipliers h0-h9 receive the sample input in an undelayed state because the multipliers are directly connected to the sample inputs 10, 11. This structure insures that the adders 13 will receive only two inputs per cycle (because of the function of the delay elements D) which eliminates the need for pipeline stages 12.

Figure 3 is an improvement to the embodiment shown in Figure 2. Rather than keeping even sample and odd sample computations separate until the final addition 14, the even and odd sample computations are combined and share the same storage elements. More specifically, with the embodiment shown in Figure 3, each of the adders 13 is placed between two multipliers (e.g., h9 and h8), one of which is connected to the even sample input 10 and the other of which is

connected to the odd sample input 11. Again, a delay element D is placed between the adders 13 to ensure that each adders 13 does not receive more than two inputs per cycle. In figure 3 there are actually 3 inputs to the adder. In Figure 3, the filter can be an interleaved non-recursive filter receiving odd and even samples, where the single adder receives an odd multiplied sample from one multiplier and an even multiplied sample from a second multiplier, depending on configuration. Figure 2 adders receive odd multiplied samples and delayed odd multiplied samples. A final adder then adds the odd and even components together. In figure 3 the above statement is correct. In Figure 2, the delay elements control the samples such that each of the adders receives at most two of the samples. For figure 3, there are 3 inputs to the adder, the delayed partial sum, a odd multiplier output, and an even multiplier output. This structure further reduces size by eliminating half of the delay devices D, when compared to the structure shown in Figure 2. The embodiment shown in Figure 3 has the same latency and approximately half the number of storage elements as the structure shown in Figure 2.

The example structure shown in Figure 1 includes 8 delay elements D each having six latches, which results in 48 total latches for the delay elements D. Each of the two overall pipeline stages includes 130 latches resulting in a total of 260 latches for the pipeline stages 12. Therefore, the example shown in Figure 1 includes a total of 308 latches.

To the contrary, to the structure shown in Figure 2 does not include any pipeline latches but instead includes 16 delay elements D each having 13 latches, resulting in a total of 208 latches. Therefore, Figure 2 reduces the total latches by 100 when compared to Figure 1. The structure shown in Figure 3 reduces the number of latches even further. More specifically, Figure 3 includes 8 delay elements D having 13 latches each and 1 delay element containing 6 latches each, which results in a total of 110 latches. Thus, the invention lowers latency (1 cycle) and uses approximately 65% less storage than conventional filters.

As discussed above, the invention reduces the size and cost of the filter by reducing the number of latches required. An additional benefit produced by the invention is a reduction in power consumption. Latches represent a large percentage of the power requirements of a filter. Since, again, the number of latches has been substantially reduced (e.g., 308 verses 110) the amount of power consumed by the inventive the filter is substantially reduced.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A non-recursive filter for receiving samples and generating a filtered signal, said filter comprising:

at least one input for receiving said samples;

a plurality of summation units, each of said summation units comprising:

at least one multiplier directly connected to said input, said multiplier multiplying said samples and providing multiplied samples; and

at least one adder connected to said multiplier, said adder adding said multiplied samples and providing added samples; and

a plurality of delay elements positioned between said summation units, said delay elements receiving said added samples and providing a delayed output of said added samples to a successive summation unit of said summation units.

2. The non-recursive filter in claim 1, wherein each of said delay elements is connected to an adder of said successive partial summation unit.

3. The non-recursive filter in claim 1, further comprising an initial delay element connected to an initial multiplier, said initial delay unit supplying an initial delayed sample to an adder of an initial summation unit.

4. The non-recursive filter in claim 1, wherein said multiplier receives said samples in an undelayed state.

5. The non-recursive filter in claim 1, wherein each of said summation units includes two of said multipliers supplying said multiplied sample to a single adder.

6. The non-recursive filter in claim 5, wherein said non-recursive filter comprises an interleaved non-recursive filter receiving odd and even samples and said single adder receives an odd multiplied sample from one multiplier and an even multiplied sample from a second multiplier.

7. The non-recursive filter in claim 1, wherein said delay elements control said samples such that each of said adders receives at most two of said samples.

8. A non-recursive filter for receiving samples and generating a filtered signal, said filter comprising:

a plurality of successive partial summation units, each partial summation unit having multiplier for multiplying an undelayed state of each of said samples, and an adder for adding multiplied samples; and

a plurality of delay elements each coupled to said adder for receiving added samples and for providing a delayed output of said added samples to a successive partial summation unit.

9. The non-recursive filter in claim 8, wherein each of said delay elements is connected to an adder of said successive partial summation unit.

10. The non-recursive filter in claim 8, further comprising an initial delay element connected to an initial multiplier, said initial delay unit supplying an initial delayed sample to an adder of an initial summation unit.

11. The non-recursive filter in claim 8, wherein said multiplier receives said samples in an undelayed state.

12. The non-recursive filter in claim 8, wherein each of said summation units includes two of said multipliers supplying said multiplied sample to a single adder.

13. The non-recursive filter in claim 12, wherein said non-recursive filter comprises an interleaved non-recursive filter receiving odd and even samples and said single adder receives an odd multiplied sample from one multiplier and an even multiplied sample from a second multiplier.

14. The non-recursive filter in claim 8, wherein said delay elements control said samples such that each of said adders receives at most two of said samples.

15. An interleaved non-recursive filter for receiving samples and generating a filtered signal, said filter comprising:

at least one input for receiving said samples;

a plurality of multipliers directly connected to said input, said multipliers multiplying said samples and providing multiplied samples;

a plurality of adders connected to said multiplier, said adders adding said multiplied samples and providing added samples; and

a plurality of delay elements positioned between said adders, said delay elements receiving said added samples and providing a delayed output of said

added samples to a successive adder of said adders.

16. The interleaved non-recursive filter in claim 15, further comprising an initial delay element connected to an initial multiplier, said initial delay unit supplying an initial delayed sample to an initial adder.

17. The interleaved non-recursive filter in claim 15, wherein said multipliers receive said samples in an undelayed state.

18. The interleaved non-recursive filter in claim 15, wherein two of said multipliers supplies said multiplied sample to each of said adders.

19. The interleaved non-recursive filter in claim 18, wherein said samples comprise odd and even samples and said single adder receives an odd multiplied sample from one multiplier and an even multiplied sample from a second multiplier.

20. The interleaved non-recursive filter in claim 15, wherein said delay elements control said samples such that each of said adders receives at most two of said samples.

INTERLEAVED FINITE IMPULSE RESPONSE FILTER

ABSTRACT

A non-recursive filter for receiving samples and generating a filtered signal, the filter comprises a plurality of successive partial summation units, each partial summation unit having multiplier for multiplying an undelayed state of each of the samples, and an adder for adding multiplied samples; and a plurality of delay elements each coupled to the adder for receiving added samples and for providing a delayed output of the added samples to a successive partial summation unit.

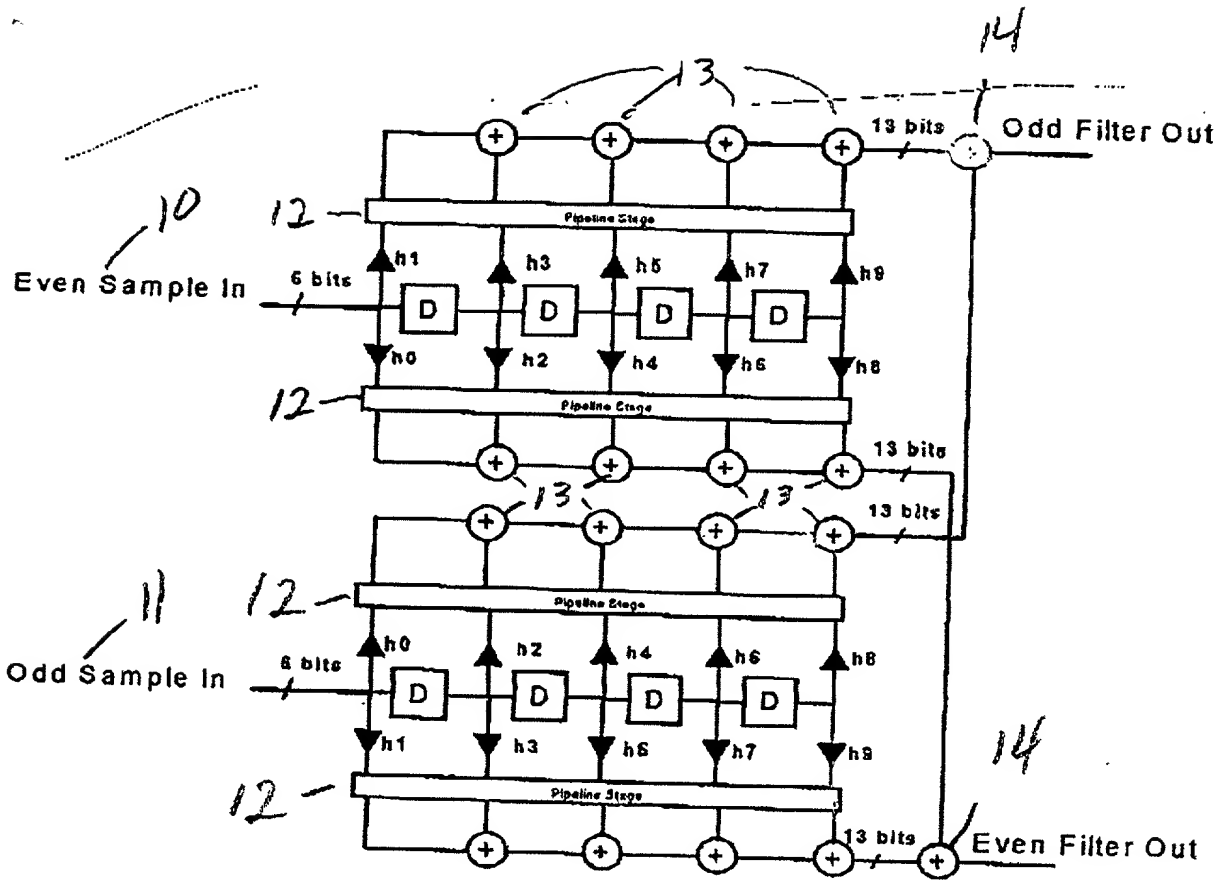


Figure1

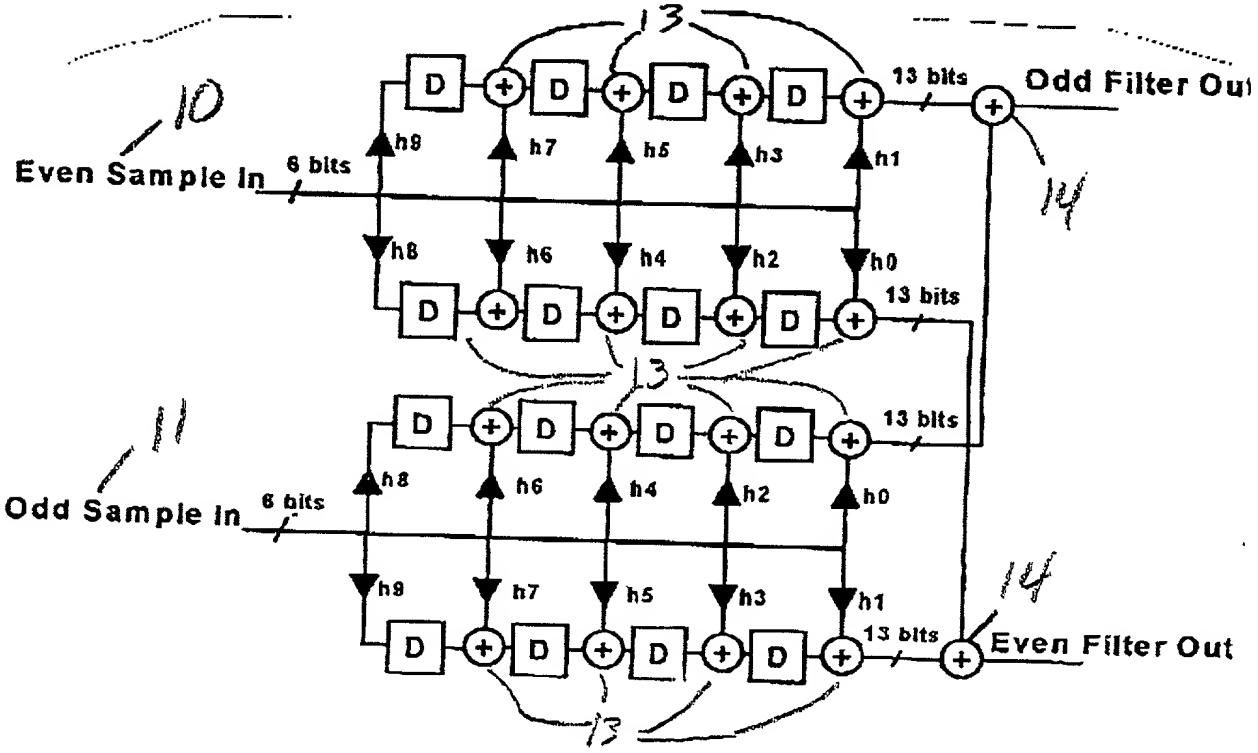
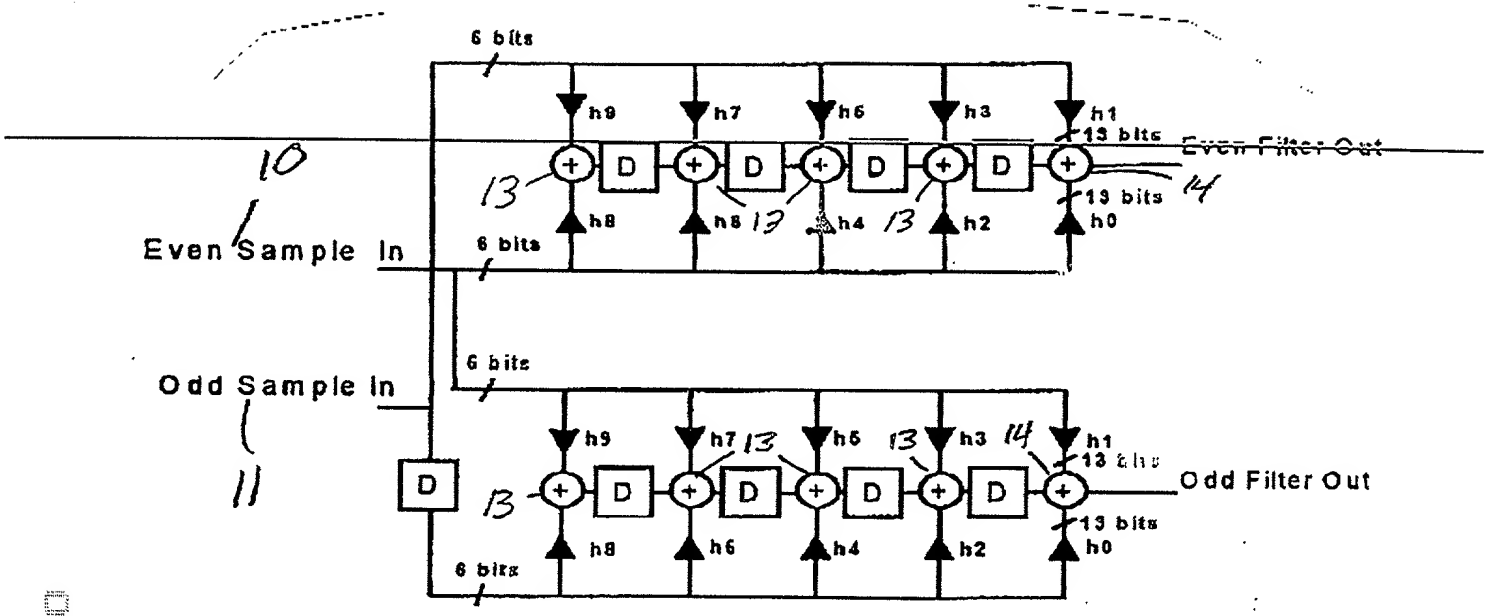


Figure 2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h9
h7
h6
h3
h1
13 bits
Even Filter Out
10
13
14
h8
h8
13
h4
13
h2
h0
13 bits
Even Sample In
6 bits
6 bits
Odd Sample In
h9
h7
13
h5
13
h3
14
h1
13 bits
11
D
13
h8
h6
h4
h2
h0
13 bits
Odd Filter Out
6 bits

Figure 3

Express Mail Label No.: EL046032163US IBM Docket No.: BUR990217US1

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: INTERLEAVED FINITE IMPULSE RESPONSE FILTER

the specification of which:
(check one)

☒ is attached hereto.
☐ was filed on _____, as Application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

Number	Country	Day/Month/Year	Priority Claimed

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

Serial No.	Filing Date	Status

I hereby declare that all statements made herein of my own knowledge are true arid that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Tide 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Mark F. Chadurjian (Reg. No. 30,739), Richard A. Henkler (Reg. No. 39,220), Richard M. Kotulak (Reg. No. 27,712), James M. Leas (Reg. No. 34,372), William D. Sabo (Reg. No. 27,465), Eugene I. Shkurko (Reg. No. 36,678), Robert A. Walsh (Reg. No. 26,516), Howard J. Walter, Jr. (Reg. No. 24,832), Christopher A. Hughes (Reg. No. 26,914), Edward A. Pennington (Reg. No. 32,588), John E. Hoel (Reg. No. 26,279), Joseph C. Redmond, Jr., (Reg. No. 18,753), Sean M. McGinn (Reg. No. 34,386), and Frederick W. Gibb, III (Reg. No. 37,629).

Send all correspondence to: **McGinn & Gibb, P.C., 1701 Clarendon Boulevard, Suite 100, Arlington, Virginia 22209, Customer No. 21254.**
Telephone calls should be directed to: McGinn & Gibb, P.C. at (703) 294-6699

(1) Inventor: Brian L. Allen
Signature: Brian L. Allen Date: 1/28/00

Residence: 7 Iroquois Ave., Essex Junction, VT 05452

Citizenship: USA

Post Office Address: Same as Residence